Intel® 852GM / 852GMV Chipset Graphics and Memory Controller Hub (GMCH)

Specification Update

November 2004

Notice: The Intel® 852GM/852GMV chipset may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

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Revision History

Revision	Description	Date
- 001	Initial Release	May 2003
- 002	Added information for 852GMV	Feb 2004
- 003	Includes Updates: • Specification Change #1 • Specification Clarification #1 • Documentation Change #1	November 2004

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Preface

This document is an update to the specifications contained in the *Intel® 852GM/852GMV Chipset GMCH Datasheet*. It is intended for hardware system manufacturers. It contains Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the Intel® 852GM/852GMV Chipset GMCH-M behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The Intel 852GM/852GMV chipset GMCH may be identified by the following register contents.

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A1	8086h	3580h	01h
A2	8086h	3580h	02h

NOTES:
The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space.
The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space.
The Revision Number corresponds to bits 7-0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel 852GM chipset GMCH may be identified by the following component markings.

Stepping	S-Spec	Top Marking	Notes
A1	SL6QG	RG82852GM	Production 82852GM GMCH
A2	SL6ZK	RG82852GM	Production 82852GM GMCH

The Intel 852GMV chipset GMCH may be identified by the following component markings.

Stepping	S-Spec	Top Marking	Notes
A2	SL742	RG82852GMV	Production 82852GMV GMCH

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Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes that apply to the listed Intel 852GM/852GMV chipset GMCH steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

Errata

NO.	Stepping		PLANS	ERRATA
	A1	A2		
1	X	X	No Fix	VGA Panning Test Issue
2	X	X	No Fix	VGA Timing issue
3	X	X	No Fix	Intermittent System hangs during power cycle test.
4	X		Fixed	PCI Compliancy WHQL failure

Specification Changes

NO.	Stepping			PLANS	SPECIFICATION CHANGES
	A1	A2			
	852GM	852GM	852GMV		
1	X	X	X		24-Bit LVDS Will Not Be Supported On 852GM/GMV Platforms

Specification Clarifications

NO.	Stepping			PLANS	SPECIFICATION CLARIFICATIONS
	A1	A2			
	852GM	852GM	852GMV		
1			X		Strapping Option Clarification

Documentation Changes

NO.	Stepping			PLANS	DOCUMENTATION CHANGES
	A1	A2			
	852GM	852GM	852GMV		
1	X	X	X		Ball Definition For RSTIN# Incorrectly Shown In Table 32

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Errata

1. VGA Panning

Problem: VGA text mode diagnostic and stress test applications that use pixel panning can experience temporary visual anomalies under certain memory configurations. This issue is seen in two test configurations.

1. Test applications using a single VGA font table with a 32KB font buffer range could fail. The failure can occur using 64MB technology products that use 2KB and 4KB page sizes. This failure was seen in a diagnostic utility.
2. Test applications using multiple VGA font tables could fail if the first two fonts are from different tables. This failing condition can occur in any memory configuration. This failure was seen in a stress test utility.

Implication: Entire scan lines will appear to flicker in some VGA diagnostic and stress test applications. However, there are no known customer sightings of this erratum. No known end user applications fail for this erratum.

Workaround: None.

Status: There are no plans to fix this erratum in silicon.

2. VGA Timings

Problem: Some VGA applications, running in 40-column modes that use a non-black border color may experience color/visual issues on systems configured with certain monitors.

Implication: 40-column VGA modes may experience visual color anomalies on some CRT monitors. This was observed using VGA focused Intel test software. With certain monitors, colors in active areas may change as the border color changes. As observed while using the test software, visual color anomalies can range from a slight color change difference to a blank screen. Based on the lack of customer or end user reported issues related to this erratum, the number of VGA applications that run in 40-column modes and also use non-black border colors is low. Based on Intel's validation and compatibility testing, the number of CRT monitors that exhibit this color anomaly is also low.

Workaround: None.

Status: There are no plans to fix this erratum in silicon.

3. Intermittent system hangs during BIOS memory testing when power cycle testing

Problem: Systems may intermittently hang during BIOS memory testing as a result of the internal RCOMP state machine colliding with BIOS induced RCOMP cycle.

Implication: System hang may occur during boot-up or resume from S3. No other failures have been identified or reported. Issues are resolved with a BIOS workaround.

Workaround: Contact your local Intel Field representative if you require BIOS workaround information.

Status: There are no plans to fix this erratum in silicon.

4. PCI compliancy WHQL failure

Problem: The WHQL PCI 2.2 compliancy test suite tests the entire PCI configuration space to verify compliance to PCI 2.2 specification. The test reads Device #2: Function #1: Register 3Dh it finds a value for this device. The test then reads Device#2: Function#1: Register 3Ch and expects a value of 00h or FFh but finds a non-zero mirrored value from Device #2: Fucntion#0: Register 3Ch indicating that an interrupt is assigned. Thus failing PCI 2.2 compliancy testing. Since interrupts are not used by function#1, the value in register 3Ch has no affect and causes no functional impact.

Implication: No functional failure. Test is failing two HCT PCI2.2 compliancy tests.

Workaround: WHQL waiver approved from Microsoft for A1 stepping.

Status: Fixed in A2.

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Specification Changes

1. 24-Bit LVDS will not be supported on 852GM/GMV platforms

Due to no availability of 24-Bit LVDS panels for validation, 24-Bit LVDS support is dropped from 852GM/GMV platforms. This change affects section 5.5.2.1 paragraph 4. Any text stating support for 24-Bit LVDS should be ignored.

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Specification Clarifications

1. Strapping Option Clarification

Notes 1, 2, and 3 have been added to Table 35, “Strapping Signals and Configuration” in Section 8.1, pg 163.

GST[2] **Note**: Intel 852GMV GMCH Only	§Clock Config: Bit_2 PSB 400 = 0 PSB 533 = 1	See notes 1, 2, 3	DVO	Hi-Z

NOTES:

1. External pull-ups/downs will be required on the board to enable the non-default state of the straps.
2. Only GST[2] is used to strap the FSB frequency to either 400MHz or 533MHz, GST0 and GST1 must be left un-strapped.
3. DDR and GFX frequencies are set by BIOS programming of the HPLLCC register (D0,F3, reg C0-C1h).

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Documentation Changes

1. Ball definition for RSTIN# incorrectly shown in Table 32

Section 7.3 Table 32, “XOR Chain Exclusion List of Pins” incorrectly shows the ball definition for RSTIN# to be D28. Actual ball definition is AD28. D28 is a VSS ball. This is the only reference where RSTIN# is incorrectly defined. Ballout and Package Information in Section 9 are correct.

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