

IDF2011
INTEL DEVELOPER FORUM

Designing for Next Generation Best-In-Class Platform Responsiveness

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Intel Chipset Components Group

EFIS004

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Agenda



- **Responsiveness Introduction**
- **2012 Technology Improvements in UEFI**
 - Active Resume BIOS Update
 - Intel® Rapid Start Technology
 - Intel® Smart Response Technology
 - Fast USB Enumeration
- **Building in Responsiveness**
- **Summary**

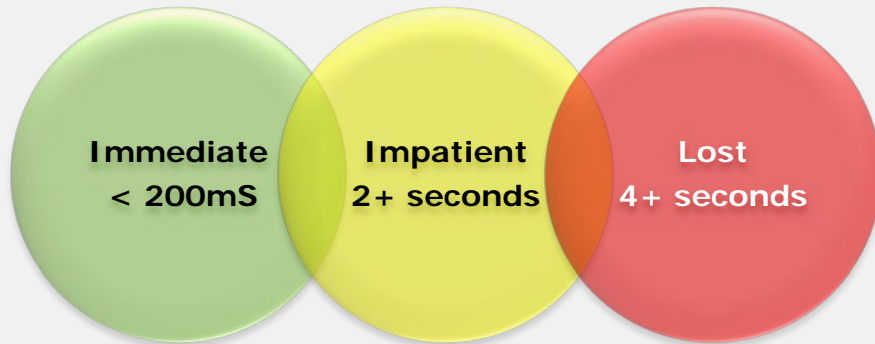
Responsiveness in BIOS?

- **Traditionally Slow boot times**
- **Longer-than-wanted resume times**
- **ACPI S-State vs. Latency Trade-offs**
- **Limiting usage models**
 - Stale Web content, Specific Target OS
- **Potential for customization**
 - Scaling the embedded point-solution up/out
 - Unmanageable code/source

Major Improvements Possible with UEFI

The Human Factor

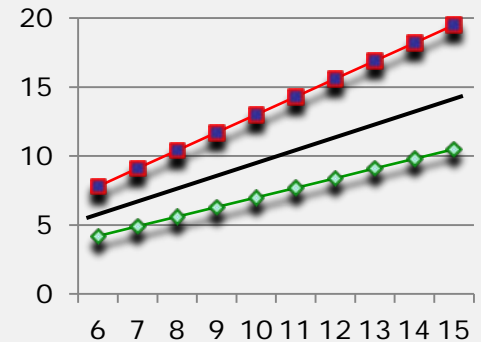
Our Brain's Perception



Miller 1968

Hard to Detect Variations

- 75% of people cannot detect change of +/- 8% between 2s and 4s
- From 0.6 to 0.8 seconds was 10% variation
- From 6 to 30 seconds, a 20-30% variation



What does this mean to developers?

**Low Power
Resume
<200-300mS**

**Splash Screen(s)
<2 seconds**

**S4/S5
Resume
<4 seconds**

Commonality across Client Segments

Tablets

Laptops

Desktops

Thin and Light

Low Power

Energy Efficient

Equally Responsive



Achieve Responsiveness with UEFI

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Active Resume BIOS Update

Usage & Benefits

System Sleep, S3



System On, S0



Power Sequence

BIOS Resume

OS Resume

Panel Timing

Benefits

- Faster S3
- Shared SEC/PEI with S4/S5 boot
- Intel® Rapid Start Technology
- Intel® Smart Connect Technology

Applies to

- Any Intel® Core CPU, Intel® 7 Series CS
- CPU Core Integrated Graphics
- UEFI BIOS

Intel 2010 Customer Reference Board - S3 Resume Experiments

Total of ~200mS spent on CPU PEI init;
65% of the total BIOS S3 resume time

GUID Description	Execution Time (mS)
Core PEI	4
CMOS Manager PEI	2
WDT App PEI	1
SB PEI	21
PCH SMBUS Arp Disabled	5
TCG PEI	1
Over clocking Init	1
NB PEI	5
PCH init PEI	2
TXT PEI	1
Memory Init	12
CPU PEI Before Mem	3
CPU PEI	204
Total time to wake vector*	~313

GUID Description	Execution Time (mS)
GetS3ResumeVariable	3
Find Microcode then copy to memory	3
StartAllAps	45
DisableAllNem	3
LoadMicrocodeOnCpus	51
EnableCacheOnCpus	84
Total	~204

* - Certain SEC routines and PEI dispatcher and other overhead may not be accounted for in table above. Dozen+ steps took less than 1mS and registered 0mS .

S3 Optimization Prototype Results

	S3 BIOS Execution Time
Starting Point	313 mS
Preliminary effort	200 mS
Final Results	85 mS*

Preliminary savings 100mS

- Moved from 33MHz to 50MHz SPI
- House Keeping per latest BIOS specs
 - Manage APs in batch mode
 - Loading MUs in parallel
 - Enabling Caches in parallel
 - Any semaphores should be 128B aligned

Final Results: <100mS

- Turn on Prefetching before uCode load
- Do not detect TPM presence more than once
- Remove unused code paths
- Shadow Setup menu variable in block read
- Use smarter AP initialization loops
- Cache CPU PEI in memory before execution

* - based on Intel CRB with specific configuration without a TPM

Active Resume BIOS provides a starting point

- **Work with your IBV to achieve optimized S3 path**
- **Request this feature from your motherboard vendor**
- **Talk to your Graphics Vendor about restart of drivers**
- **Talk to your OS vendor about Resume time, Panel Timing request**
- **Talk to your Panel Vendor about minimizing backlight timings**



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Intel® Rapid Start Technology

Usage & Benefits

System Sleep, S4/S5



<5 Second

System On, S0



Power Sequence

BIOS Resume / Memory Restore

OS Resume

Panel Timing

Benefits

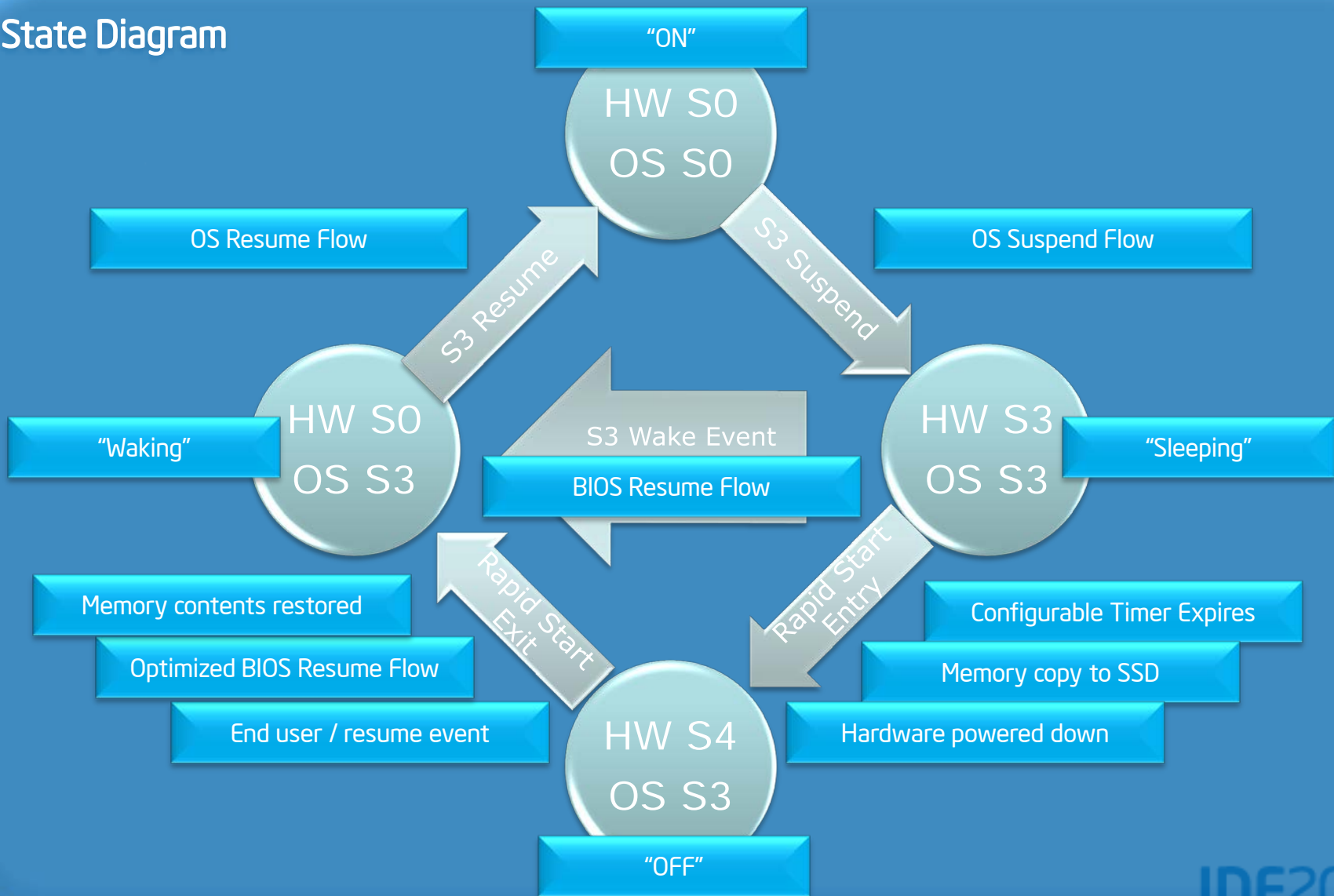
- Replaces OS hibernate function with BIOS function
- HW Powers down to S5 state
- OS resumes back as if from S3

Requirements

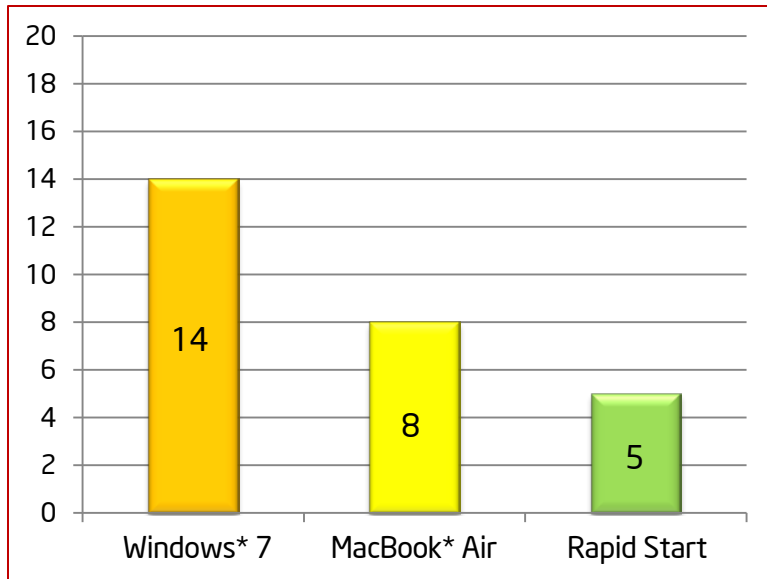
- UEFI BIOS with Intel UEFI Ref Code
- Private SSD partition equal to memory size
- Special Partition Table entry into GPT
- Additional ACPI hooks and security precautions for SSD/SMRAM.

Intel® Rapid Start Technology Overview

State Diagram

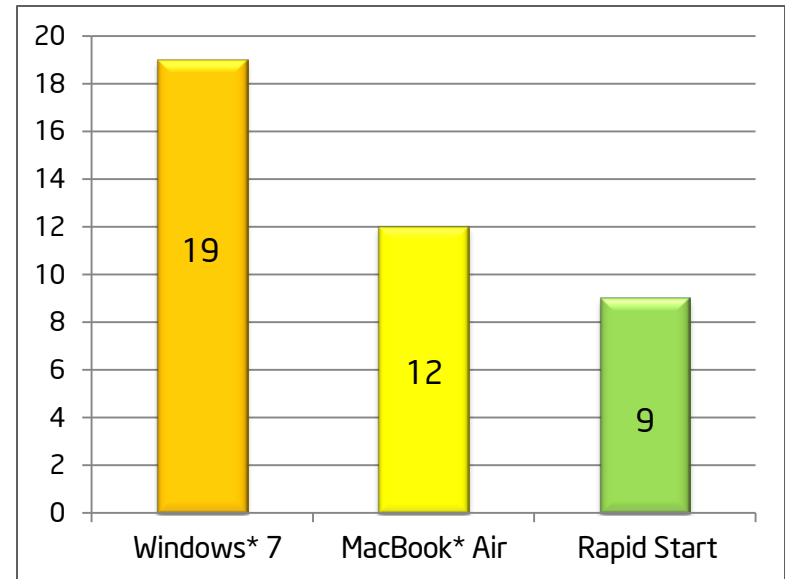


S0 Resume - Intel® Rapid Start Technology compared to Windows* 7 and MacBook* Air



Idle

1.6 to 2.8 times Faster



Loaded

1.3 to 2.1 times Faster

Notes/Source:

All data is based on SATA2 SSD. Performance may vary per device generation and current workload.

Windows* 7 - Intel reference platform, Windows*7 OS, Intel® Core™ i5 CPU, 4GB of memory, Intel® Series 6 Chipset. OS hibernate resume

MacBook* Air - MC505LL/A 11", 4 GB 1066 MHz DDR3, 1.4GHz Core™ 2 Duo, after sleeping for greater than 70 minutes

Rapid Start - Win7 Hardware with Intel® Rapid Start Technology applied

Intel® Rapid Start Technology Summary

- Improves Existing OS boot time experience
- Saves power and battery life over S3
- Performance can vary with:
 - SSD data-readiness time
 - SATA generation of drive/controller
 - OS Application Load
- Works with and Complements:
 - Active Resume BIOS Update
 - Intel® Smart Connect Technology
 - Intel® Smart Response Technology

Contact your BIOS vendor
UEFI Reference code available under NDA through Intel Field

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Intel® Smart Response Technology



- Combines capacity of HDD with speed of an SSD
- Two storage devices look like a single device to the OS and user
- Uses standard (SATA) ports for both drives.

Benefits

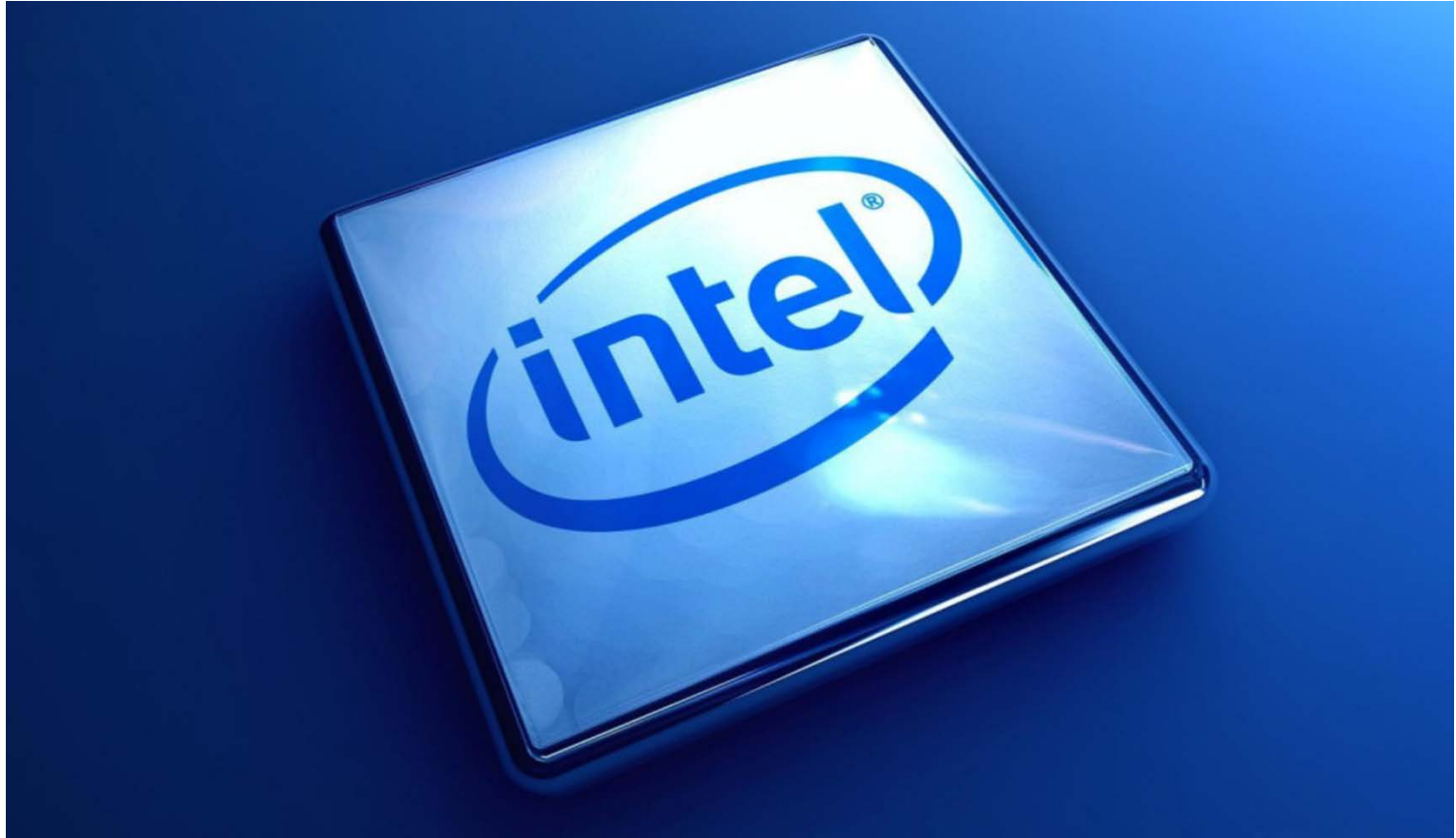
- High Performance - System Boots and Applications load with SSD-like performance
- Less Cost - than large capacity SSD
- Large Capacity - equal traditional HDD
- Lower Power - avoids spinning up HDD as often

Requirements

- Intel® 6 & 7 Series Chipset supporting RAID (i.e. H77, Z77, Q77, Z68)
- Both SSD and HDD installed and active
- SATA-connected SSD of at least 20GB
- mSATA port is optional but provides small space for SSD upgrade option
- Requires the RAID Legacy Option ROM or UEFI driver to be supported in BIOS

Intel® Smart Response Technology

Demo



Intel® Smart Response Technology Summary

- Improves Existing OS boot time and runtime experience
- Saves power by using primarily SSD and leaving HDD spun down
- Performance can vary with:
 - SATA generation of drive/controller
- Works with and Complements:
 - Intel® Smart Connect Technology
 - Intel® Rapid Start Technology

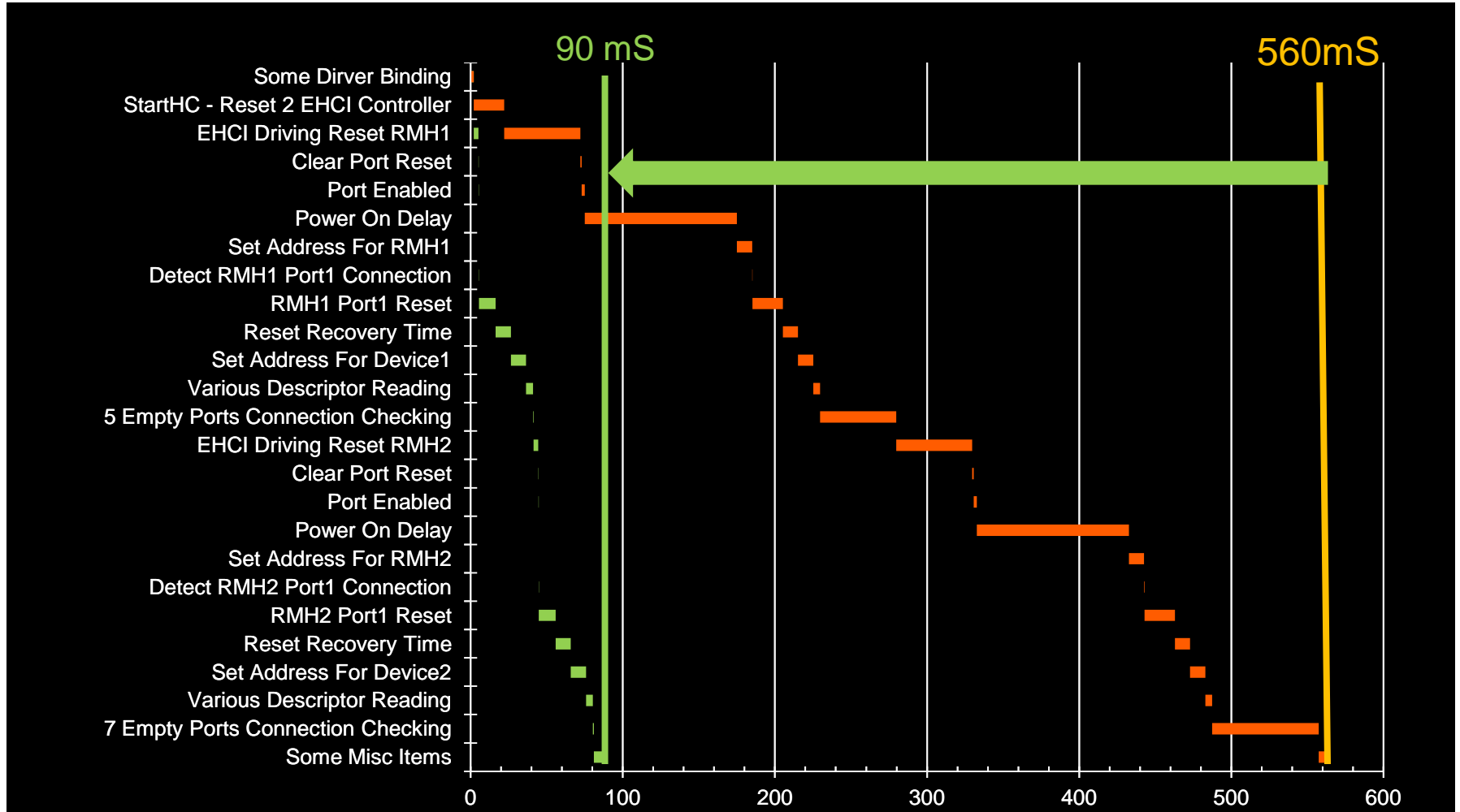
Intel® 6 & 7 Series Chipsets with support this capability
(ie. H77, Z77, Q77, Z68)

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USB2 Enumeration Timing*



2 USB HID Devices < 100mS

- Based on Intel reference platform, Intel® Core™ i5 processor with Intel® Series 6 chipset.
- Performance varies per number or type of USB devices

How?

Optimizations	Savings (ms)	Notes
Skip Power On delay	200	RMH ports are powered from the motherboard. No power on delay needed. 100mS per RMH saved.
Optimal RMH Ports Reset handling	118.8	Only perform reset if device connected.
EHCI driving shorter reset to RMH. Instead of driving the reset signal for 50ms, do so for 3ms	94	But continue to drive 50ms reset signal in warm reset path. Possible to have 2 RMH reset at parallel
Fine Grain Polling on Ports	23	First a delay of 10ms, then followed by fine grain polling at 90us. Normally seeing reset complete within 10-11ms. Still make sure the fine grain polling cover another 10ms range for specification compliance. This time includes Finer grain polling on port reset clear (1.5mS), and Finer grain polling on port enable (3.8mS)
Skip EHCI Controller Reset	20	Intel RC reset EHCI controller in DXE
Skip SetAddress recovery interval for RMH	20	Intel integrated RMH does not need this
Savings for 2 devices	475.8	

- Performance varies per number and type of USB devices
- Based on Intel customer reference platform Intel® Core i5 processor with Intel® Series 6 chipset
- Above applies for EHCI, XHCI will be optimized as the technology and products mature.

Agenda



- Responsiveness Introduction
- 2012 Technology Improvements in UEFI
- **Building in Responsiveness**
 - Motherboard
 - Hardware Components
 - OS
 - UEFI/BIOS
 - Developers
- Summary

Factors Effecting Boot Speed

- **Hardware Power Planes and Power Sequencing**
 - Provide Separate Power Plane for ME
 - Specify tighter than 100mS PCI Spec delay for Power Supplies
 - Shorten Power Button De-bounce in Embedded Controllers
 - Specify Display Panel timing to what the HW is capable of, not specification
- **Storage Solution Selection**
 - SSD > 2x faster than HDD
 - SSD Data Readiness timing
 - SATA2 vs. SATA3
- **SPI**
 - Higher Frequency is better
 - Number of Bytes per Read

Build the motherboards for speed

Talk with your Suppliers

Select the right parts

Factors Effecting Boot Speed

- **Processor**
 - Higher Frequency is better
 - Less No. of Cores/Threads is faster boot, but slower runtime performance
- **Main Memory**
 - Higher Frequency is better
 - Less No of Banks is faster boot, but slower runtime performance
- **Video & Graphics**
 - Controller & Panel Timings important
 - UEFI Graphic Output Protocol driver is faster
 - Single Graphics solution is faster
- **Security**
 - Trusted Platform Module will add time
 - Secure & Measured Boots will add time
- **Platform Features**
 - More Complex the solution, the longer it may take to boot (RAID example)
 - Remote Boot enabled and checked will affect boot

Work with your IHVs

Be aware of trade offs

Factors Effecting Boot Speed

- **OS Needs/Requirements**
 - Reduce OS Image Size
 - Enable User Interface sooner
 - Needing Keyboard as a boot device
- **Enable Class 3 UEFI Solution**
 - No CSM support
- **Tool used to measure speed**
 - Injects delays if not done properly
 - Methods may vary per tool used
- **Security**
 - Trusted Platform Module will add time
 - Secure & Measured Boots will add time
- **Platform Features**
 - More Complex the solution, the longer it may take to boot (RAID example)
 - Remote Boot enabled and checked will affect boot

Work with your IHVs

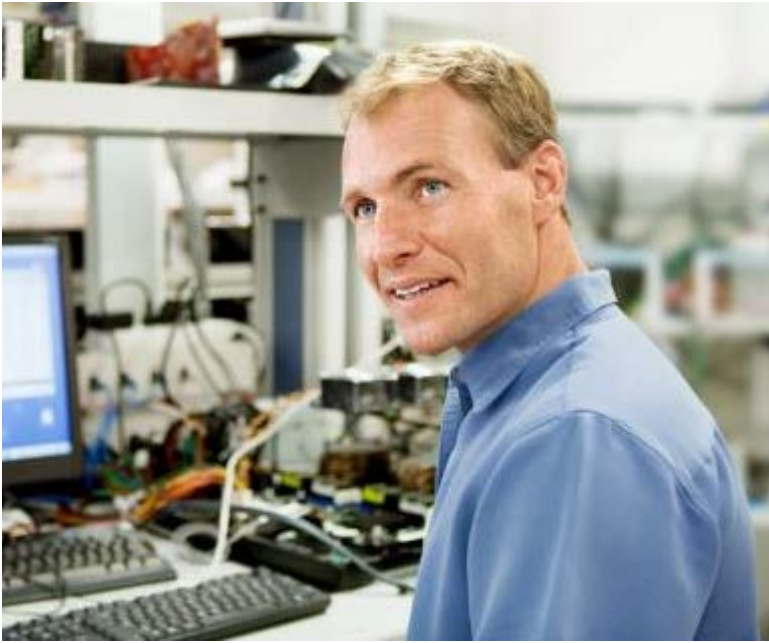
Be aware of trade offs

Factors Effecting Boot Speed

- **A Pessimistic Mentality in System Developers**
 - “It’s only a few Milliseconds”
 - “S3 is fast enough”
 - “It’s a systemic problem”
 - “Even if the BIOS disappears, the OS is still slow”

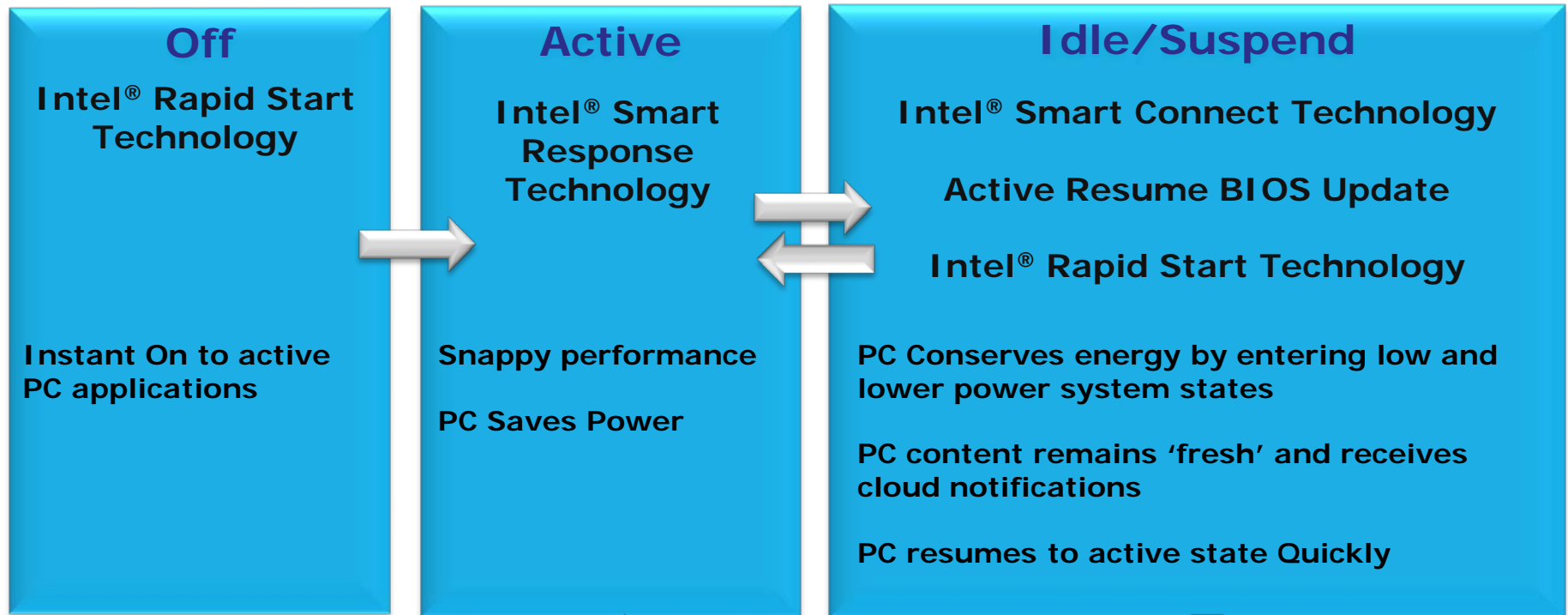
Don't Ignore YOUR role in Responsiveness

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Intel 2012 Responsiveness Technologies: Improves User Experience



**UEFI Intelligent Infrastructure
makes these technologies happen**

Summary

- **Rethink your PC-AT based assumptions about Responsiveness**
- **Build in Complementary Responsiveness Technologies**
 - Active BIOS Resume Update
 - Intel® Rapid Start technology
 - Intel® Smart Response Technology
 - Intel® Smart Connect Technology
- **Drive Responsiveness from your HW & UEFI Layers up**
- **Achieve a more responsiveness with UEFI**

Start Today !

Q&A

Tunnel Mountain Intel DQTM57 UEFI 2.3.1 platform

Intel® UDK 2010 Compatible, supports UEFI 2.3.1

Pre-assembled systems available at HDNW, visit

<http://www.Tunnelmountain.net>

tomk@hdnw.com, (425) 943-5515 ext 42234. Use product name "Tunnel Mountain" when ordering



Comes with class 2 CSM and UEFI enabled firmware
Download site has Class 3 UEFI only firmware(nocsm)

Comes with serial port for debug
Can be ordered with optional ITP connector and
socketed SPI flash - AC-SPEC4480

Visit <http://developer.intel.com/technology/efi/uefi-ihv.htm> for
the latest information and other IHVs collateral

Fall 2011 UEFI Plugfest – Taipei, Oct 24-27



UEFI FALL 2011 OCTOBER 24-27 TAIPEI
UEFI PLUGFEST
Hosted by Insyde Software

We'll See You There!

Visit www.UEFI.org for Event Info & Registration

UEFI Industry Resources

UEFI Forum

Welcome What's New: UEFI Specifications Update!

- UEFI Specification**: Current UEFI Spec: v2.3 approved May, 09. Current Activities: Implementation and writer's guides.
- UEFI Shell Specification**: Current Shell Spec: v2.0, approved Oct, 08. Current Activities: Implementation support.
- PI Specification**: Current PI Spec: v1.2, approved May, 09. Current Activities: Implementation support.
- UTWG self-test Specification**: Current version: SCTv2.1 released May, 09. Next Release: v2.3 SCT target mid 2010.
- PI Distribution Package Specification**: Current version: v1.0 released May, 09. Current Activities: Implementation support.

www.uefi.org

UEFI Open Source

SourceForge.net: tianocore - Windows Internet Explorer

Introducing UDK2010
Beginning a new era for the UEFI Open Source Community

Welcome to the UEFI Open Source Community Master project. This project is the gateway to all open source projects associated with Intel's support of UEFI specifications, through the Platform Innovation Based environment for running pre-boot applications and for booting an operating system. It specifies the layer between an operating system and the platform firmware.

Sub-projects	Summary	Sourceforge project URL	Download
EDK2-fat-driver	EDK-fat-driver	http://sourceforge.net/projects/eds2-fat-driver	Download
EDK2-fat-driver	EDK-fat-driver	http://sourceforge.net/projects/eds2-fat-driver	Download

www.tianocore.org

Intel UEFI Resources

Extensible Firmware Interface (EFI) and Unified EFI (UEFI)

Defining the interface between the operating system and platform firmware

Background

The Unified EFI (UEFI) Specification (previously known as the EFI Specification) defines an interface between an operating system and platform firmware. The interface consists of data tables that contain platform-related information, boot service calls, and runtime service calls that are available to the operating system and its loader. These provide a standard environment for booting an operating system and running pre-boot applications.

The UEFI Specification was primarily intended for the next generation of IA architecture-based computers, and is an outgrowth of the "next" boot initiative (NBI) program that began in 1998.

Intel's original version of this specification was publicly named EFI, ending with the EFI 1.10 version.

In 2005, The Unified EFI Forum was formed as an industry-wide organization to promote adoption and continue the development of the EFI Specification. Using the EFI 1.10 Specification as the starting point, this industry group released the following specifications, renamed Unified EFI.

The current version of the UEFI Specification can be found at the UEFI web site.

Specifications

UEFI Specifications
The latest version of the UEFI Specification is available from the UEFI web site.

EFI Specifications
Learn more and download specification documents.

Tools and utilities

www.intel.com/technology/efi/index.htm

Intel EBC Compiler

Intel® C Compiler for EFI Byte Code

All prices listed below are Manufacturer Suggested List Prices (MSRP) and include Taxes (VAT) or any other state or local taxes or charges.

Customers with 10 or more licenses qualify for the Intel® Volume Program. Learn more about the benefits of this program.

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Intel® C Compiler for EFI Byte Code

What's Included

Full product:

- New user license and media for Intel® C Compiler for EFI Byte Code
- Technical notes, documentation, and more
- One year of support services, which includes technical support (Intel® Premier Support) upgrades and new releases during that term

<http://software.intel.com/en-us/articles/intel-c-compiler-for-efi-byte-code-purchase/>

UEFI Books

Harnessing the UEFI Shell
Moving the platform beyond BIOS

Beyond BIOS:
Developing with the Unified Extensible Firmware Interface

www.intel.com/intelpress

Training/IHVs Contact

Laurie Jarlstrom

- Intel UEFI Training
- Laurie.Jarlstrom@intel.com

Brian Richardson

- Intel IHVs UEFI Support
- Brian.Richardson@intel.com

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UEFI Sessions Moscone SF IDF 2011

Session ID	Title	Company	Day / Time	Rm
✓ EFIS001	UEFI Security and Networking Advancements	Intel & Insyde SW	Tue 1:05 – 1:55	2009
✓ EFIS002	UEFI Innovations for Platform Security	Intel & AMI	Tue 2:10 - 3:00	2009
✓ EFIS003	Beyond DOS: UEFI Modern Pre-boot Application Development Environment	Intel & Phoenix Tech. LTD	Tue 3:20 - 4:10	2009
✓ EFIS004	Designing for Next Generation Best-In-Class Platform Responsiveness	Intel	Tue 4:25 - 5:15	2009
EFIQ001	Hot Topic Q&A: UEFI in the Industry	All Speakers	Tue 5:25 - 6:00	2009
EFIS005	Microsoft* Windows* Platform Evolution and UEFI Requirements	Intel & Microsoft	Thu 1:05 - 1:55	2005
SPCQ003	Hot Topic Q&A: Intel & Microsoft - Windows * 8	Intel & Microsoft	Thu 2:05 - 2:55	2005

✓ = DONE

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- All products, dates, and figures specified are preliminary based on current expectations, and are subject to change without notice.
- Intel, processors, chipsets, and desktop boards may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are available on request.
- Other code names featured are used internally within Intel to identify products that are in development and not yet publicly announced for release. Customers, licensees and other third parties are not authorized by Intel to use code names in advertising, promotion or marketing of any product or services and any such use of Intel's internal code names is at the sole risk of the user
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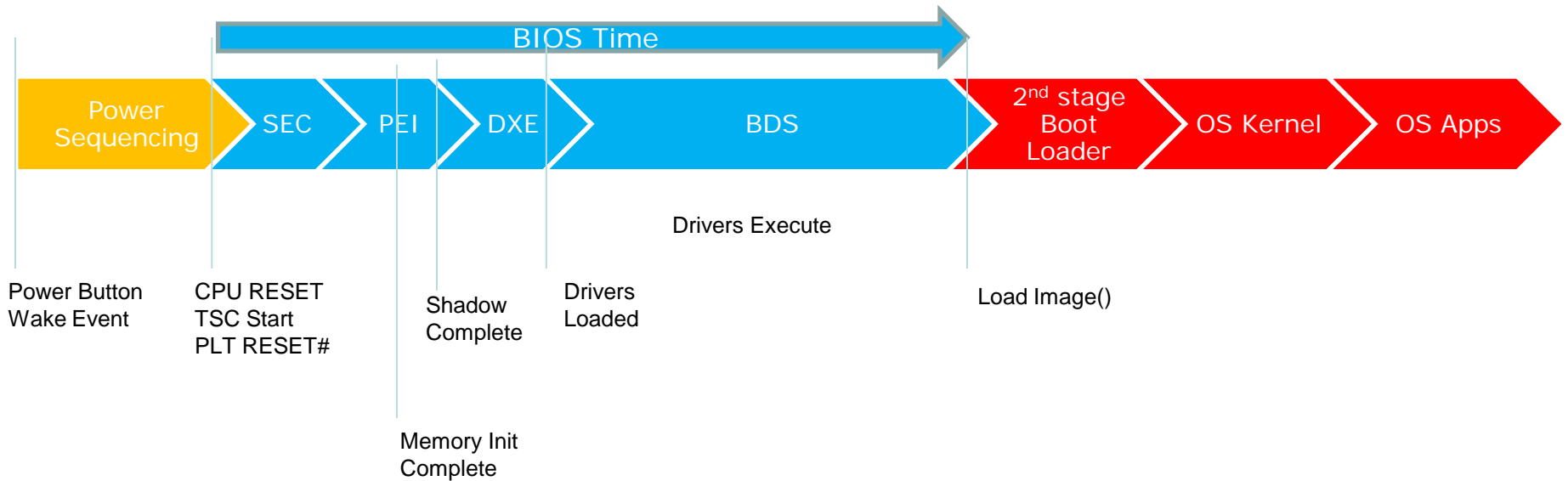
Rev. 5/9/11

Agenda



Backup

Typical Power on Flow Button to Browse



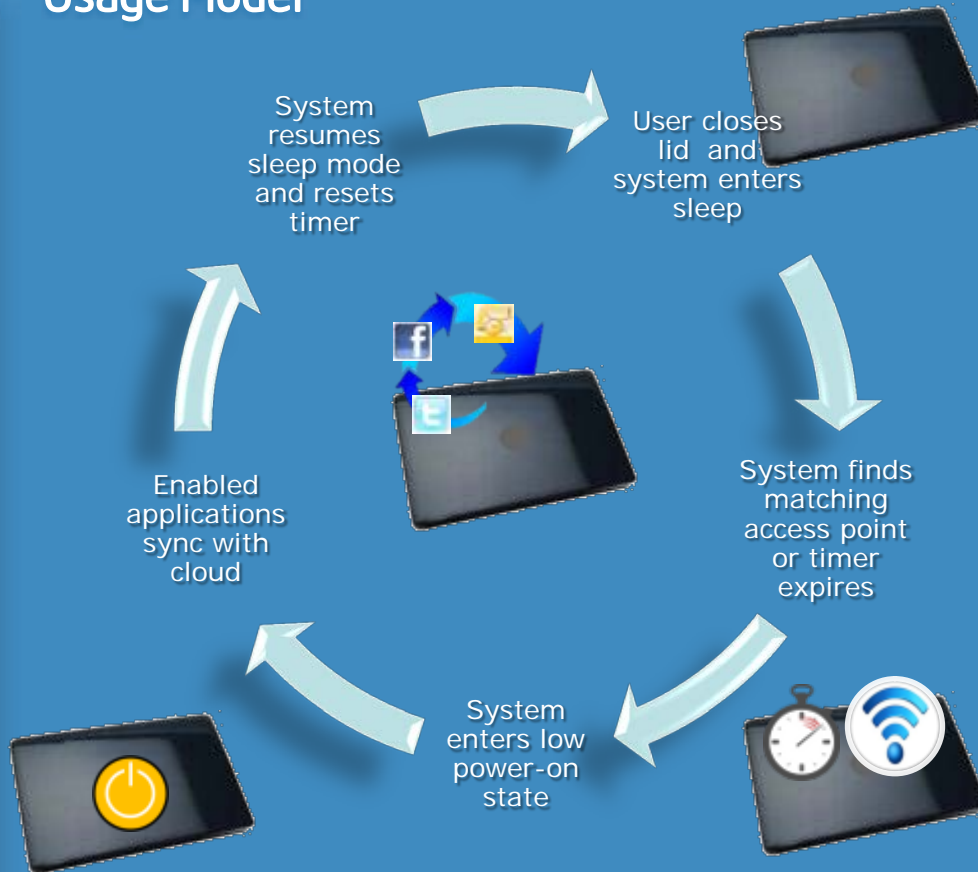
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Intel® Smart Connect Technology

Usage Model



Benefits

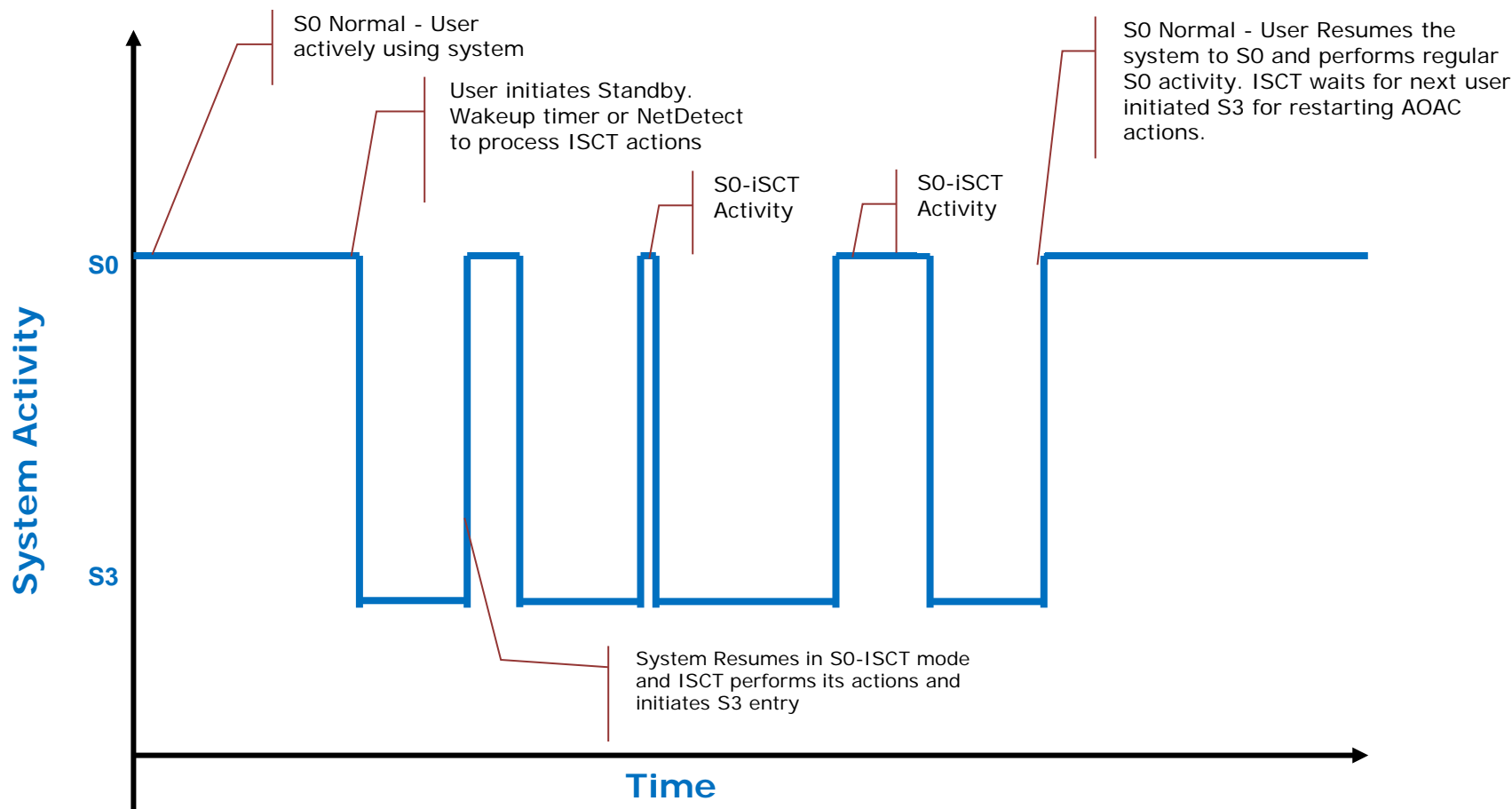
- Desired content is already updated on the system when user wants it
- Content on the system synchronizes with the cloud service, no manual interaction
- Quicker access to internet, data and applications

Intel® Smart Connect Technology

BIOS Requirements

- **New Intel Smart Connect Technology ACPI pseudo device object:**
 - Toggle Feature On/Off
 - Toggle Notification (LED alerts, etc)
 - Indication of active periodic wakes
 - Toggle Power to WLAN (or WWAN) Module in Sleep, Hibernate, or Intel® Rapid Start Technology
 - Set RTC upon entrance to S3
 - Enables proper Platform Wake Events (EC, Power Button, RTC)
- **Enable system to wake via WLAN**
- **Disable RTC wakes from S4 (OS Hibernate)**
 - RTC wakes only to be cleared when BIOS is requested by OS to enter S4

Intel® Smart Connect Technology State Change Example



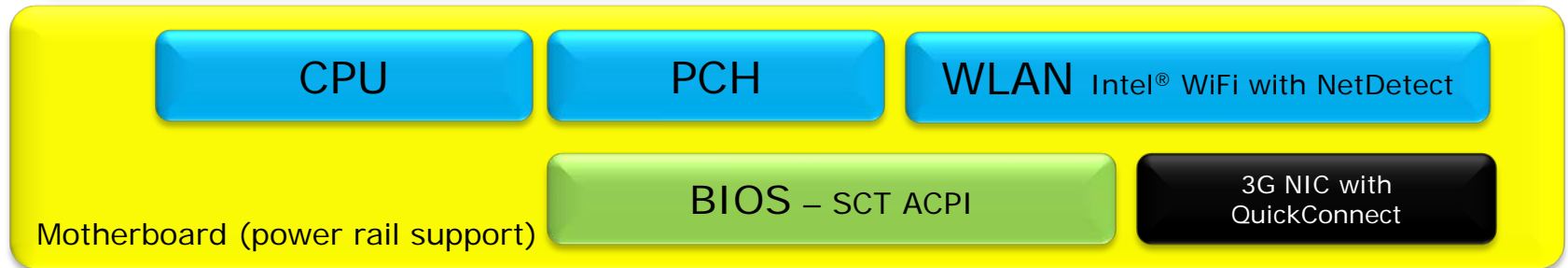
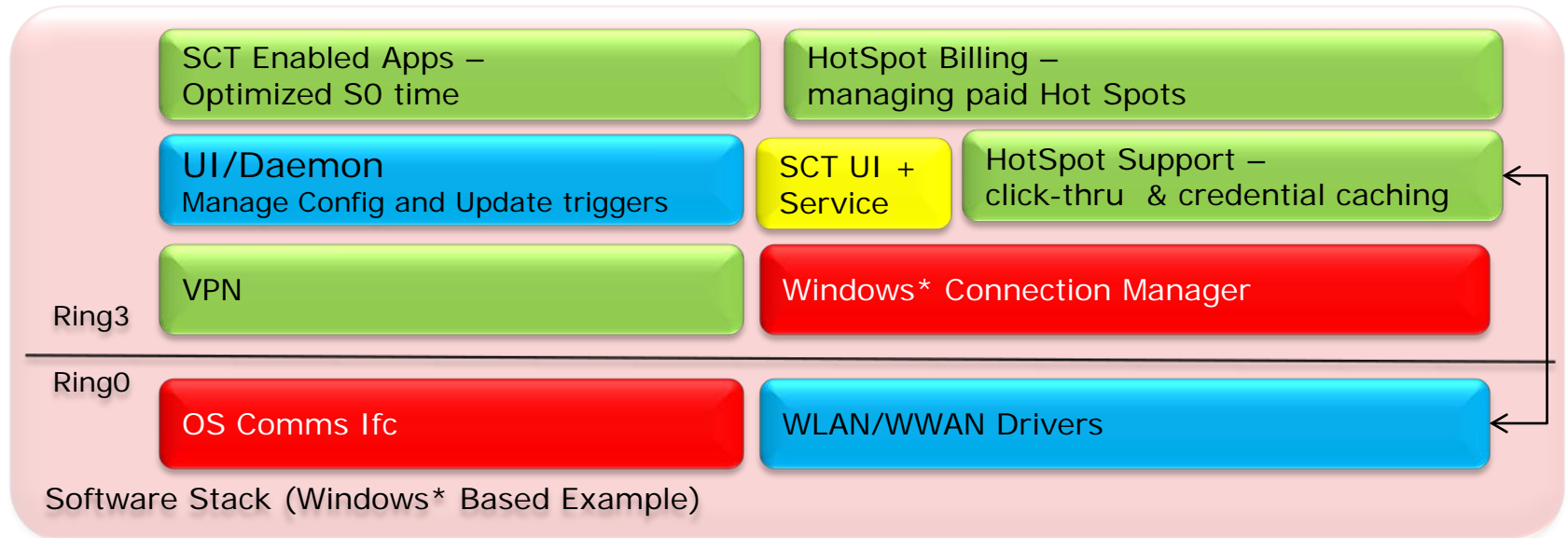
Intel® Smart Connect Technology is a new Usage Model

- A new Usage model that improves runtime experience with fresh data on resume
- Performance/Feature benefits enhanced with:
 - SSD installed vs. an HDD
 - Intel® Smart Response Technology
 - Intel® Rapid Start Technology
 - Active Resume BIOS Update
 - Better OS & Application resume and suspend time
- Ask your BIOS vendor and Software Vendor about support

Contact your Intel Field Sales representative
for more information

Platform Architecture Overview

Intel® Smart Connect Technology (SCT)



Complete solution stack delivering seamless connectivity experience



Intel Smart Connect Technology ACPI Extensions

Control Method	Description
GABS	Get Intel Smart Connect Technology BIOS Enabled Setting
GAOS / SAOS	Get/Set Intel Smart Connect Technology Function Status
GANS / SANS	Get/Set Intel Smart Connect Technology Notification Status
GWLS / SWLS	Get/Set WLAN Module Status
GWWS / SWWS	Get/Set WWAN Module Status
SASD	Set Intel Smart Connect Sleep Duration
GPWR	Get Platform Wake Reason

Agenda

A blurred photograph of two people walking in a hallway. The person on the left is wearing a light blue jacket and dark pants, carrying a folder. The person on the right is wearing a grey sweater and dark pants, also carrying a folder. The background shows a hallway with blue doors and a tiled floor.

UEFI BIOS Start &
Finish Line

A blurred photograph of a server room. The image shows a long row of dark server racks with glass doors. The floor is tiled, and the ceiling has recessed lighting. The overall scene is dimly lit, emphasizing the rows of equipment.

Time Measurement at “Finish Line”

- Starting line is CPU RESET exit
- Finish Line is “start of call to LoadImage() on the successful boot target”
 - Same for built-in EFI shell or EFI Boot Manager (x64 Windows)
 - Keep logging all LoadImage() for multiple boot targets
 - Report the LoadImage() call of the 1st successful boot target image as BDS end-point
 - INT19 is equivalent to “connect to device with the image to load”
 - Close to LoadImage() of the successful OS load
- TSL (Transient System Load) phase overlaps with OS Loader
 - TSL phase is described in the Framework as the time before the final OS environment
 - TSL phase starts when BDS phase ends
 - TSL phase ends when ExitBootServices() is called (regardless if INT19 legacy interface is used or not)
- DP64.efi will show BIOS boot time as SEC+PEI+DXE+BDS
 - TSL time will be shown but not counted towards BIOS Boot Time
 - TSL time + BIOS Boot time will give us closer number compared to Xperf (Windows) tool view of BIOS POST time.