

# **Intel® Xeon® Processor E7- 2800/4800/8800 v2 Product Family**

**Boundary Scan Descriptor Language (BSDL) Readme**

---

*February 2014*



INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. Intel products are not intended for use in medical, life saving, life sustaining, critical control or safety systems, or in nuclear facility applications.

A "Mission Critical Application" is any application in which failure of the Intel Product could result, directly or indirectly, in personal injury or death. SHOULD YOU PURCHASE OR USE INTEL'S PRODUCTS FOR ANY SUCH MISSION CRITICAL APPLICATION, YOU SHALL INDEMNIFY AND HOLD INTEL AND ITS SUBSIDIARIES, SUBCONTRACTORS AND AFFILIATES, AND THE DIRECTORS, OFFICERS, AND EMPLOYEES OF EACH, HARMLESS AGAINST ALL CLAIMS COSTS, DAMAGES, AND EXPENSES AND REASONABLE ATTORNEYS' FEES ARISING OUT OF, DIRECTLY OR INDIRECTLY, ANY CLAIM OF PRODUCT LIABILITY, PERSONAL INJURY, OR DEATH ARISING IN ANY WAY OUT OF SUCH MISSION CRITICAL APPLICATION, WHETHER OR NOT INTEL OR ITS SUBCONTRACTOR WAS NEGLIGENT IN THE DESIGN, MANUFACTURE, OR WARNING OF THE INTEL PRODUCT OR ANY OF ITS PARTS.

Intel may make changes to specifications and product descriptions at any time, without notice. The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an order number and are referenced in this document, or other Intel literature may be obtained by calling 1-800-548-4725 or by visiting Intel's website at <http://www.intel.com/design/literature.htm>.

Intel, Xeon, and the Intel logo are trademarks of Intel Corporation in the U.S. and/or other countries.

\*Other names and brands may be claimed as the property of others.

Copyright © 2014, Intel Corporation. All Rights Reserved.



# Table of Contents

---

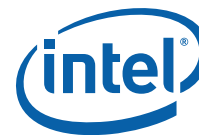
<b>Table of Contents</b> .....	3
<b>Overview</b> .....	5
Scope .....	5
Related Documents .....	5
<b>Readme</b> .....	6
Full Boundary-Scan .....	6
Partial Boundary-Scan .....	6
<b>Tables</b>	
1 BSDL File Summary .....	5
2 Related Documents .....	5
<b>Figures</b>	
1 Reset Sequence .....	7



## Revision History

---

Document Number	Revision Number	Description	Date
329598	001	<ul style="list-style-type: none"><li>Initial Release</li></ul>	February 2014



# Overview

## Scope

This document is intended for the development of IEEE 1149 Boundary Scan Tests for the Intel® Xeon® Processor E7-2800/4800/8800 v2 Product Family. This Readme assumes a working knowledge of IEEE 1149 methodologies and the In Circuit Test (ICT) manufacturing test methods.

This release package supports the processor steppings shown in the table below.

**Table 1. BSDL File Summary**

<ul style="list-style-type: none"> <li>• IVB_EX_D1.bsdI</li> <li>• IVB_EX_C0.bsdI</li> <li>• IVB_EX_B3.bsdI</li> <li>• IVB_EX_B0.bsdI</li> <li>• IVB_EX_A0.bsdI</li> </ul>	Full Boundary Scan File
<ul style="list-style-type: none"> <li>• IVB_EX_D1_partial.bsdI</li> <li>• IVB_EX_C0_partial.bsdI</li> <li>• IVX_EX_B3_partial.bsdI</li> </ul>	The respective BSDL files with a shortened boundary-scan chain due to the excluded Intel® Scalable Memory Interconnect (Intel® SMI) 2 pins
<ul style="list-style-type: none"> <li>• IVB_EX_BSCAN_INIT.txt</li> </ul>	The initialization sequence needed to enable partial BSCAN operation.

## Related Documents

Refer to the following documents for additional processor information.

**Table 2. Related Documents**

Document	Document Number/Location
IEEE Standard Test Access Port and Boundary Scan Architecture Specification	<a href="http://standards.ieee.org">http://standards.ieee.org</a>



# Readme

---

## Full Boundary-Scan

After applying voltage to the power pins, the following initialization sequence must be completed prior to TAP accesses during application of the boundary-scan test patterns:

- a. BCLK[1:0]\_D[P/N] continuous toggle at 100 MHz
- b. VMSE\_PWR\_OK, PWRGOOD, RESET\_N are initialized LOW.
- c. All power supplies are up.
- d. VMSE\_PWR\_OK is driven HIGH and remains driven HIGH for the duration of the boundary-scan test pattern execution
- e. EAR\_N pin is initialized HIGH.
- f. PROCHOT\_N pin is initialized HIGH.
- g. EAR\_N and PROCHOT\_N need to be initialized HIGH (de-asserted) prior to PWRGOOD assertion
- h. PWRGOOD pin must be driven HIGH 2 ms after power pins are stable and remain drive HIGH for the duration of the boundary-scan test pattern execution.
- i. RESET\_N pin should be driven LOW for the duration of the boundary-scan test pattern execution.

## Partial Boundary-Scan

The partial boundary-scan is necessary due to a known issue with the Intel® Xeon® Processor E7-2800/4800/8800 v2 Product Family which is described below:

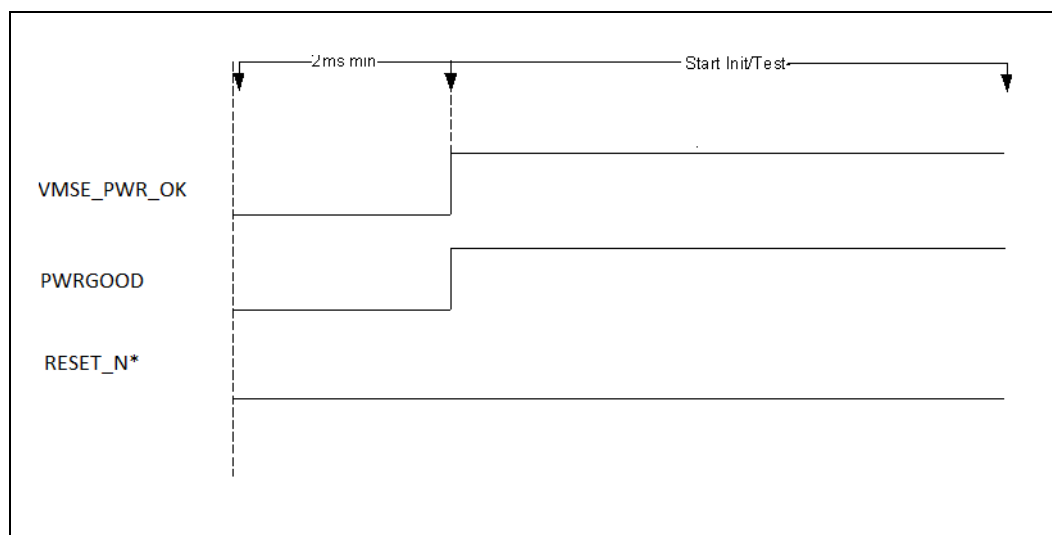
**Problem:** A full function Boundary-scan operation requires a continuous running BCLK[1:0], however in some cases a partial BSDL file is needed where a continuous BCLK is not supplied. Also, The processor has limitation where if a full reset sequence is not applied, the PCU will not power up the Intel® Scalable Memory Interconnect (Intel® SMI) 2 domain so Intel SMI2 Boundary Scan is not available.

**Implication:** In cases where designs cannot do full a power-on during board manufacturing, the boundary-scan operation can cover all other pins with the partial BSDL file and the initialization sequence from the IVB\_EX\_BSCAN\_INIT.txt file.

**Workaround:** A workaround to this is to enable Partial Boundary-scan functionality. If a continuous BCLK[1:0] cannot be supplied, BSCAN functionality can still be enabled with the exception of the Intel SMI2 pins. To enable this mode, the initialization sequence described below needs to be applied prior to the boundary-scan operation.

After applying voltage to power pins, the following initialization sequence must be completed prior to the first TAP accesses during application of the boundary scan test patterns:

- a. VMSE\_PWR\_OK, PWRGOOD, RESET\_N are initialized low.
- b. All power supplies are up.
- c. VMSE\_PWR\_OK is driven HIGH and remains driven HIGH for the duration of the boundary-scan test pattern execution.
- d. PWRGOOD pin must be driven HIGH 2 ms after power pins are stable and remain driven HIGH for the duration of the boundary-scan test pattern execution.
- e. RESET\_N pin should be driven LOW for the duration of the boundary-scan test pattern generation.

**Figure 1. Reset Sequence**

§

